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RISC-V Microconference

The RISC-V software eco-system is gaining momentum at breakneck speed with three new Linux development platforms available this year. The new platforms bring new issues to deal with. One of the pressing issues is the handling of non-coherent systems as two of the three new platforms have non-coherent devices. We would like to continue the RISC-V MC platform to discuss these issues with a wider community to arrive at a solution as we have done in the past. In the past, these discussions have been very fruitful resulting in several major milestones including but not limited to Glibc upstreaming for RV32[1], RISC-V platform specification improvements[2] [3], ongoing EBBR support for RISC-V[4] while some of the features such as KVM is yet to be merged[5].

Here are a few of the expected topics and current problems in RISC-V Linux
land that we would like to cover.

- Platform specification progress, including SBI-0.3 https://github.com/riscv/riscv-sbi-doc/releases/tag/v0.3.0 and the future plans for SBI-0.4. There has been significant progress on the platform specifications, including a server profile, that needs discussion https://github.com/riscv/riscv-platform-specs.
- Privileged specification progress, possible 1.12 (which is a work in progress at the foundation).
- Support for the V https://github.com/riscv/riscv-v-spec and B https://github.com/riscv/riscv-bitmanip specifications, along with questions about the drafts. The V extension is of particular interest, as there are implementation of the draft extensions that are likely to be incompatible with what will eventually be ratified so we need to discuss what exactly user ABI compatibility means.
- H extension / KVM discussion, which is probably part of the drafts. The KVM port has been hung up on the H extension ratification process, which is unlikely to proceed any time soon. We should discuss other options for a KVM port that avoid waiting for the H extension.
- Support for the batch of SOCs currently landing (JH7100, D1)
- Support for non-coherent systems
- How to handle compliance, now that we're on the hook

Possible participant list:

- Palmer Dabbelt
- Atish Patra
- Kumar Shankaran
- Guro Ren
- Drew Fustini
- Anup Patel
- Nick Kossifidis
- Paolo Bonzini
- Arnd Bergman
- Al Stone

Come join us and participate in the discussion on how we can improve
the support for RISC-V in the Linux kernel.

MC Runners: Atish Patra atish.patra@wdc.com, Palmer Dabbelt palmerdabbelt@google.com

[1] https://sourceware.org/pipermail/libc-announce/2021/000030.html
[2] https://lists.riscv.org/g/tech-unixplatformspec/message/1042
[3] https://github.com/riscv/riscv-platform-specs/blob/main/riscv-platform-spec.adoc
[4] https://lists.linaro.org/pipermail/boot-architecture/2021-May/001822.html
[5] https://lwn.net/Articles/856685/

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