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Status of Dual Stage SMMUv3 integration

Monday, 9 September 2019 15:30 (25 minutes)

Since August 2018 I have been working on SMMUv3 nested stage integration at IOMMU/VFIO levels, to allow virtual SMMUv3/VFIO integration.

This shares some APIs with the Intel and ARM SVA series (cache invalidation, fault reporting) but also introduces some specific ones to pass information about guest stage 1 configuration and MSI bindings.

In this session I would like to discuss the upstream status and get a chance to clarify open points. This is also an opportunity to synchronize about the VFIO fault reporting requirements for recoverable errors.

I agree to abide by the anti-harassment policy

Yes

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